# Autovectorization in LLVM

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July 21, 2014







- Basic Flow of Loop Vectorization
- Loop Legalizer Requirements and Examples

SIMD Streaming Extension and Advanced Vector eXtension are SIMD extensions for the  $x86/x86_{-}64$  architecture.

Overview over the history

- MMX 64 bit MM-registers, for 64,32,16 and 8 bit integers
- SSE Adds 128 bit XMM-registers for floats
- SSE2 XMM registers may be used for integers and doubles
- SSE3/4 More operations like max/min, mostly for graphics
- AVX Adds 256 bit YMM-registers, only for floats and doubles

Analogous instructions exist for ARM, PPC and other architectures. GPUs are based on the SIMD Model.

### LLVM Compilation Flow



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  - Often reruns analyses and transformations multiple times
  - Can be printed with -debug-pass=Arguments
- Many have (implicit) prerequisites (i.e. loop vectorizer)

# LLVM Intermediate Language (IL)

- Primitive Types float i1 i32 i8\*
- Vector Types <N x T> for vector length N, primitive type T
- Instructions that work on primitive types

%x = add i32 %a, %b

also work on vectors

%y = add <4 x i32> %v1, %v2

• Vector values are mapped to SIMD registers on target machine

Goals:

- Unroll loops for less overhead
- Use SIMD instructions to process multiple data at once

$$\begin{aligned} a_1 &:= b_1 \odot c_1 \\ \vdots \\ a_n &:= b_n \odot c_n \end{aligned} \Rightarrow \begin{pmatrix} a_1 \\ \vdots \\ a_n \end{pmatrix} &:= \begin{pmatrix} b_1 \\ \vdots \\ b_n \end{pmatrix} \odot \begin{pmatrix} c_1 \\ \vdots \\ c_n \end{pmatrix} \\ SISD \qquad SIMD \end{aligned}$$

- Sometimes usage of multiple processors
- Linearizing Control Flow (Also called flattening)

### Basic flow of Loop Vectorization in LLVM



Figure: Basic Loop Vectorization Flow

### Structural Vectorization of Loops



Figure: Original Loop

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Figure: Vectorized Loop

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In short: Determines how to vectorize the loop

- Only vectorizes innermost loop (innermost-loop.c)
- Strides of exactly 1 (non-one-strides.c)
- IL needs to be optimized beforehand (needs-preoptimization.c)
- Division within the loop (may trap, division-in-loop.c)
- C++-class induction/reduction fails (IntegerWrapper.cpp)

### Requirement - Single Backwards edge



Figure: Two Backward Edges, Loop of multiple-backward-edges.c

## Requirement - Single Unique Exit



Figure: Two distinct exit nodes, Loop of different-exit-blocks.c

Despite all this, LLVM is still a good choice for Loop Vectorization:

Figure: Comparison of vectorization performance for GCC, Clang and Intel C Compiler



- LLVM Source: LoopVectorize.cpp See http: //llvm.org/doxygen/LoopVectorize\_8cpp\_source.html
- http://llvm.org/docs/Vectorizers.html
- Code examples from https://gcc.gnu.org/projects/ tree-ssa/vectorization.html