Performance Modeling and Tweaking with the Roofline Model

Case Study in Matrix-Matrix Multiplication

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High-Performance and Automatic Computing

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Agenda

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Performance Models

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- Possible tweaks should be shown by the model

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- Different levels of parallelism need to be exploited on new architectures (Task-Level Parallelism, Instruction Level Parallelism)
- Helps to evaluate if a given change to a system or application offers performance benefits before implementing it

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Roofline Model

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- Shows hardware performance limitations for a given kernel
- Shows the benefit of a few optimizations

Audience

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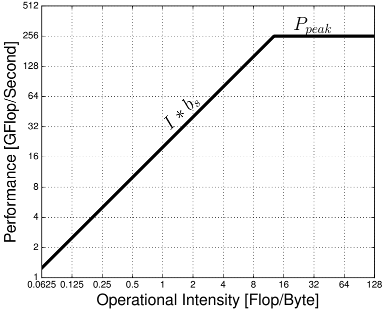
- Not for people interested in fine tuning, only gives general advices

Roofline Model



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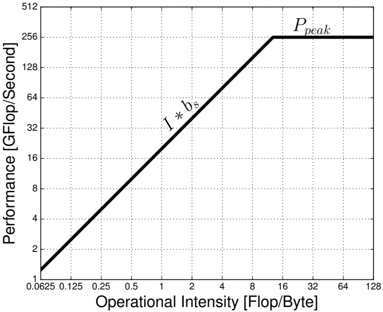

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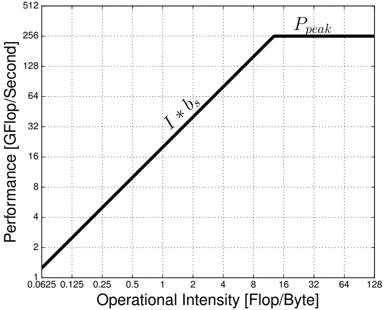

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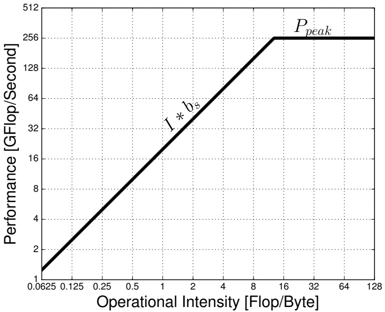

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- P_{peak} is the peak performance of the processor (F/s)
- b_s is peak bandwidth of the architecture (B/s)
- I is the computational intensity of the kernel (F/B)

How to obtain those values?

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  - ➔ Cycles per second
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- Measure memory bandwidth with the STREAM benchmark
- Calculate Operational Intensity from the algorithm

Hardware Used

Name	CPU Model	Clock Speed	Cores	SIMD	FMA	Bandwidth	Performance
MPI-S	Intel Westmere X5675	3.07 GHz	2x6	SSE	No	40 GB/s	
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- Home: 3.10 GHz $*$ 4 cores $*$ 2 $*$ 8 (2 4-wide FMA instructions) $=$ 198.4 GFlops

Naive Matrix-Matrix Multiplication

```
for (i=0; i<N; i++)
  for(j=0; j<N; j++)
    for (k=0; k<N; k++)
      res[i][j] += mul1[i][k] * mul2[k][j];
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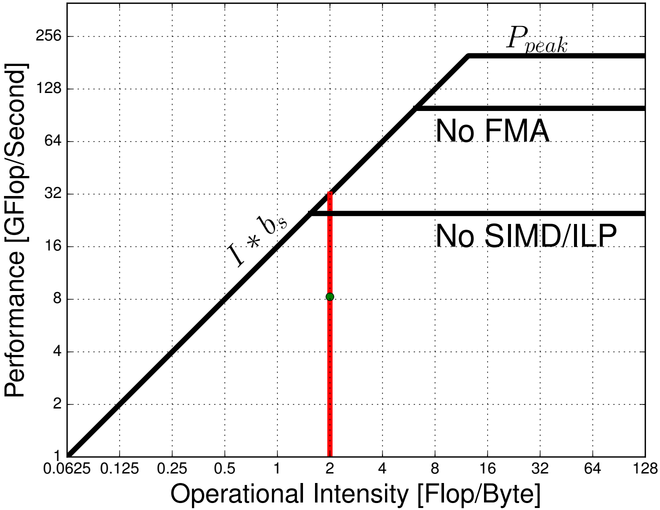
Horrible performance, do not use if performance is relevant

Highly optimized libraries available for linear algebra operations

Roofline Model for naive Matrix-Matrix Multiplication



Tiled Matrix-Matrix Multiplication

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for (i = 0; i < N; i += b)
  for (j = 0; j < N; j += b)
    for (k = 0; k < N; k += b)
      for (i2 = 0; i2 < b; ++i2)
        for (k2 = 0; k2 < b; ++k2)
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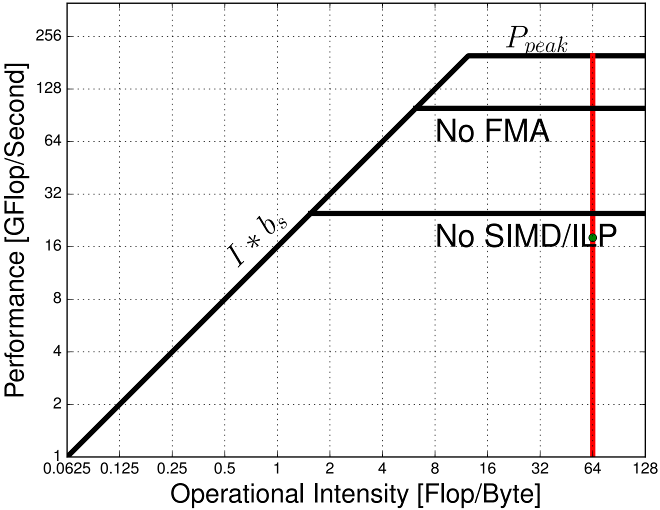
- Each block of mul1 and mul2 moves N times
- Better performance, but still much slower than tuned libraries

Roofline Model Tiled Matrix-Matrix Multiplication



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- Haswell microarchitecture allows 2 AVX instructions per cycle

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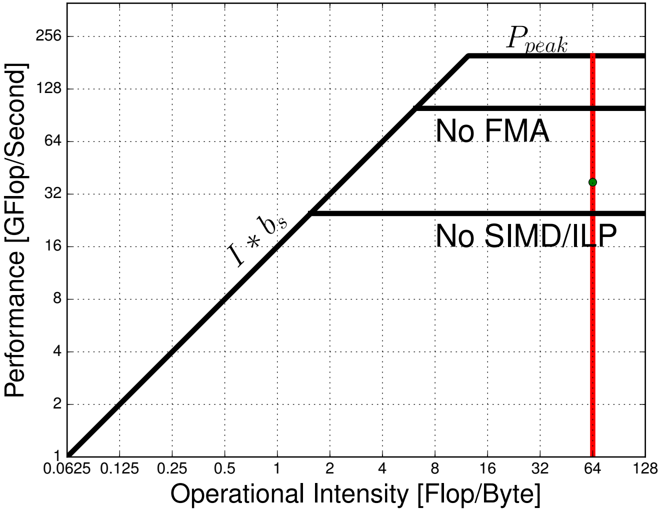
- Without using SIMD a factor 2 for SSE and factor 4 for AVX is lost

Roofline Model SIMD Optimization



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- The result is only rounded once, i.e. result is more accurate

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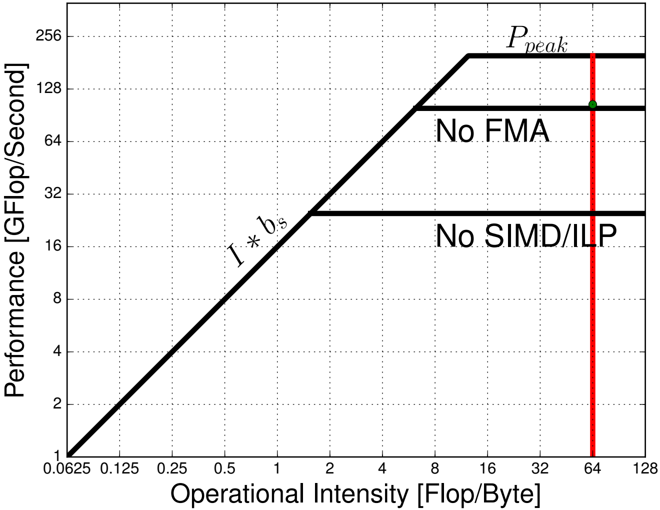
Fused Multiply–Add Optimization

- Peak performance only attainable, if algorithm uses a well balanced mix of additions and multiplications
- If only additions or only multiplications are used, a factor 2 of performance will be lost

Roofline Model Fused Multiply-Add optimization



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- Creating a Roofline Model in a few simple steps
- Compute-bound and memory-bound algorithms
- Optimizing compute-bound code using the Roofline Model

References

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