# Parallel Programming WS15 HOMEWORK #7

Submit by email to: `fabregat@aices.rwth-aachen.de`
Due by: Monday, January 4th, 5pm.

## Caches

1. Consider an application that requests the following sequence of memory blocks: `1, 4, 6, 4, 7, 4, 7, 9, 3, 5, 2, 5, 7, 4, 8, 4, 2, 5, 7, 4, 5, 2, 1, 5, 2, 7`. Assume a memory hierarchy consisting of main memory and one level of cache, where the cache has room for 4 cache blocks. With an initially empty cache, what is the status of the cache after each of the requests if we have a

   a) direct mapped cache

   b) fully associative cache

   c) set associative cache with 2 sets of 2 blocks each.

   Indicate also whether each access is a *cache hit* or a *cache miss*.

   Both caches b) and c) use "Least-recently used" as block replacement policy.

**a) Direct mapped cache**

| **Request** | 1 | 4 | 6 | 4 | 7 | 4 | 7 | 9 | 3 | 5 | 2 | 5 | 7 | 4 | 8 | 4 | 2 | 5 | 7 | 4 | 5 | 2 | 1 | 5 | 2 | 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Hit/Miss** | M | M | M | H | M | H | H | M | M | M | M | H | M | H | M | M | H | H | H | H | H | H | M | M | H | H |
| **Block 0** | | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[8] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] |
| **Block 1** | M[1] | M[1] | M[1] | M[1] | M[1] | M[1] | M[1] | M[9] | M[9] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[1] | M[5] | M[5] | M[5] |
| **Block 2** | | | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] |
| **Block 3** | | | | | M[7] | M[7] | M[7] | M[7] | M[3] | M[3] | M[3] | M[3] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] |

**b) Fully associative cache**

| **Request** | 1 | 4 | 6 | 4 | 7 | 4 | 7 | 9 | 3 | 5 | 2 | 5 | 7 | 4 | 8 | 4 | 2 | 5 | 7 | 4 | 5 | 2 | 1 | 5 | 2 | 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Hit/Miss** | M | M | M | H | M | H | H | M | M | M | M | H | M | M | M | H | M | M | M | H | H | H | M | H | H | M |
| **Block 0** | M[1] | M[1] | M[1] | M[1] | M[1] | M[1] | M[1] | M[9] | M[9] | M[9] | M[9] | M[9] | M[7] | M[7] | M[7] | M[7] | M[7] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] |
| **Block 1** | | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] |
| **Block 2** | | | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[3] | M[3] | M[3] | M[3] | M[3] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[7] |
| **Block 3** | | | | | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[2] | M[2] | M[2] | M[2] | M[8] | M[8] | M[8] | M[8] | M[7] | M[7] | M[7] | M[7] | M[7] | M[1] | M[1] | M[1] |

**c) 2-way set associative cache**

| **Request** | 1 | 4 | 6 | 4 | 7 | 4 | 7 | 9 | 3 | 5 | 2 | 5 | 7 | 4 | 8 | 4 | 2 | 5 | 7 | 4 | 5 | 2 | 1 | 5 | 2 | 7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Hit/Miss** | M | M | M | H | M | H | H | M | M | M | M | H | M | H | M | H | M | H | H | H | H | H | M | H | H | M |
| **Block 0** | | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] | M[4] |
| **Block 1** | | | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[6] | M[2] | M[2] | M[2] | M[2] | M[8] | M[8] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] | M[2] |
| **Block 2** | M[1] | M[1] | M[1] | M[1] | M[1] | M[1] | M[1] | M[9] | M[9] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] | M[5] |
| **Block 3** | | | | | M[7] | M[7] | M[7] | M[7] | M[3] | M[3] | M[3] | M[3] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[7] | M[1] | M[1] | M[7] |