Parallel Programming WS15 HOMEWORK #7

Submit by email to: `fabregat@aices.rwth-aachen.de`
Due by: Monday, January 4th, 5pm.

Caches

1. Consider an application that requests the following sequence of memory blocks: `1, 4, 6, 4, 7, 4, 7, 9, 3, 5, 2, 5, 7, 4, 8, 4, 2, 5, 7, 4, 5, 2, 1, 5, 2, 7`. Assume a memory hierarchy consisting of main memory and one level of cache, where the cache has room for 4 cache blocks. With an initially empty cache, what is the status of the cache after each of the requests if we have a

   a) direct mapped cache

   b) fully associative cache

   c) set associative cache with 2 sets of 2 blocks each.

   Indicate also whether each access is a *cache hit* or a *cache miss*.

   Both caches b) and c) use "Least-recently used" as block replacement policy.

   Example.

   Below, you find as an example the first two accesses for case a). Please, use a similar format for your answers.

   a) Direct mapped cache

   (1) Request 1: Miss

Block	Data
0	
1	`MEM[1]`
2	
3	

   (2) Request 4: Miss

Block	Data
0	`MEM[4]`
1	`MEM[1]`
2	
3	